Claims

| l | 1. A dual gate oxide high-voltage semiconductor device, comprising: |
|----------------------------------------------|----------------------------------------------------------------------------------|
| 2 | a buried oxide layer formed over a semiconductor substrate; |
| 3 | a silicon layer formed over the buried oxide layer; |
| 4 | a top oxide layer formed over the silicon layer; |
| 5 | a first gate oxide formed over the silicon layer adjacent the top oxide |
| 6 | layer; and |
| 7 | a second gate oxide formed over a portion of the first gate oxide. |
| 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 | 2. The device of claim 1, wherein the silicon layer comprises a source region, a |
| 2 | body region, and a drift region. |
| | 3. The device of claim 2, wherein the first gate oxide is formed over the drift |
| 2 = | region, the body region, and the source region. |
| 1 | 4. The device of claim 2, wherein the second gate oxide is formed over the first |
| 2 | gate oxide between the top oxide layer and the body region. |
| 1 · | 5. The device of claim 1, further comprising a field plate formed over the top |
| 2 | oxide layer, the first gate oxide, and the second gate oxide. |
| | |

- 6. The device of claim 1, wherein the first gate oxide has a thickness in a range of approximately 300-600A, and wherein the second gate oxide has a thickness in a range of approximately 900-1200A.
- 7. The device of claim 1, wherein the first gate oxide has a length of approximately 3-4 μ m, and wherein the second gate oxide has a length of approximately 1-2 μ m.

| 1 | 8. A dual gate oxide high-voltage semiconductor device, comprising: |
|-------|------------------------------------------------------------------------------------|
| 2 | a buried oxide layer formed over a semiconductor substrate; |
| 3 | a silicon layer formed over the buried oxide layer, wherein the silicon |
| 4 | layer comprises a source region, a body region, and a drift region; |
| 5 | a top oxide layer formed over the silicon layer; |
| 6 | a first gate oxide formed over the silicon layer adjacent the top oxide |
| 7 | layer; and |
| 8 === | a second gate oxide formed over a portion of the first gate oxide between |
| 8 | the top oxide layer and the body region. |
| 1 | 9. The device of claim 8, further comprising a field plate formed over the top |
| 1 | oxide layer, the first gate oxide and the second gate oxide. |
| 1 | 10. The device of claim 8, wherein the first gate oxide has a thickness in a range |
| 2 | of approximately 300-600A, and wherein the second gate oxide has a thickness in |
| 3 | a range of approximately 900-1200A. |
| 1 | 11. The device of claim 8, wherein the first gate oxide has a length of |
| 2 | approximately 3-4µm, and wherein the second gate oxide has a length of |
| 3 | approximately 1-2μm. |

| 12. The device of claim 8, wherein a thickness of approximately 1200A for the |
|--------------------------------------------------------------------------------------------------------|
| second gate oxide results in an increase from approximately 1e ¹² cm ⁻² to |
| approximately 2e ¹² cm ⁻² for a maximum allowable charge, and wherein a decrease |
| of approximately 30% for a specific-on-resistance, of the device. |

| 1 | 13. A method for forming a dual gate oxide high-voltage semiconductor device, |
|-------------------------------------------------|------------------------------------------------------------------------------------|
| 2 | comprising: |
| 3 | forming a buried oxide layer over a semiconductor substrate; |
| 4 | forming a silicon layer over the buried oxide layer; |
| 5 | forming a top oxide layer over the silicon layer; |
| 6 | forming a first gate oxide adjacent the top oxide layer over the silicon |
| 7 | layer; and |
| 1 2 3 4 5 5 5 5 5 5 6 6 7 6 7 6 7 6 7 6 7 6 7 6 | forming a second gate oxide over the first gate oxide. |
| 1 4 | 14. The method of claim 13, wherein forming the first gate oxide, and forming the |
| 2 | second gate oxide comprises: |
| 3 | growing the first gate oxide adjacent the top oxide layer over the silicon |
| 4 | layer; |
| 5 | applying a mask over the first gate oxide; and |
| 6 | growing the second gate oxide over a portion of the first gate oxide. |
| | |
| 1 | 15. The method of claim 13, wherein forming the silicon layer comprises forming |
| 2 | a silicon layer having a source region, a body region, and a drift region over the |
| 3 | buried oxide layer. |

| 1 | 16. The method of claim 15, wherein forming the first gate oxide comprises |
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| 2 | forming a first gate oxide over the drift region, the body region, and the source |
| 3 | region. |
| | |
| 1 | 17. The method of claim 15, wherein forming the second gate oxide comprises |
| 2 | forming a second gate oxide over the first gate oxide between the top oxide layer |
| 3 | and the body region. |
| | |
| 1 | 18. The method of claim 13, further comprising: |
| 2 = | increasing a maximum allowable charge of the device from |
| 3 45 | approximately $1e^{12}$ cm ⁻² to approximately $2e^{12}$ cm ⁻² ; and |
| 2 | decreasing a specific-on-resistance of the device by approximately 30%. |
| | |
| 1 | 19. The method of claim 13, wherein forming the first gate oxide and forming the |
| 2 | second gate oxide comprises: |
| 3 | forming a first gate oxide having a thickness in a range of approximately |
| 4 | 300-600A adjacent the top oxide layer over the silicon layer; and |
| 5 | forming a second gate oxide having a thickness in a range of |
| 6 | approximately 900-1200A over the first gate oxide. |
| | |
| 1 | 20. The method of claim 13, further comprising forming a field plate over the top |
| 2 | oxide layer, the first gate oxide, and the second gate oxide. |